Title:

Current Control and Monitoring for High Quality Porous Silicon Optics

Author:

Yang Lit PHAY
(20140851)

Supervisor:

Dr. Adrian KEATING

This thesis is submitted in partial fulfilment of the requirements for the degree of Bachelor of Engineering with Honours in Electrical and Electronic Engineering at the University of Western Australia.

October 2009
Professor David Smith  
Faculty of Engineering, Computing and Mathematics  
The University of Western Australia (M017)  
35 Stirling Highway  
CRAWLEY WA 6009

Dear Sir,

I cordially submit to you this dissertation entitled “Current Control and Monitoring for High Quality Porous Silicon Optics”, supervised by Dr. Adrian Keating, in partial fulfilment of the requirement of the award of Bachelor of Engineering.

Yours sincerely.

Yang Lit PHAY
Abstract

Conventional DC anodisation methods to produce porous silicon (PS) have been shown to have imperfections such as porosity gradients and interface roughness which adversely affects the performance of PS optical filters.

In order to overcome these issues, a pulsed current source has been designed, built and analysed. It has been demonstrated through a series of resistive load tests that this current source unit is capable of producing the necessary current waveforms of higher quality and bandwidth than those which have previously been shown to minimise PS imperfections.

In order to better understand the formation of pores in PS, a high speed and high precision electrochemical potential monitoring unit was also designed and constructed. This unit acts in conjunction with the pulsed current source to provide real-time anodisation voltage characterisation.

A host controller has also been developed which coordinates data communication between a host PC and the peripheral units: the pulsed current source and a gantry unit which is being built by another final year student. The host controller has also been designed to provide automation facilities which will facilitate the production of complex multilayered PS structures which are suitable to optical applications, while maximising the ability to reproduce the results.

Optical modelling software was also developed to analyse the effects of reducing porosity gradients and interface roughness. This allows analysis of the effects of reducing porosity gradients and interface roughness and thus offering insight into the improvements which can be realised when using pulsed current anodisation in the production of porous silicon as opposed to using DC anodisation.
Acknowledgements

First and foremost, I would like to acknowledge the invaluable and extensive contributions of Dr. Adrian Keating as the supervisor of this project upon whose work the modelling software was based and whose time and efforts have made this project possible.

Many thanks to PhD candidate David Wyndham for his extremely valuable advice in the design of the systems and software developed in this project. Many thanks also to final year project student Jason Moore for his design advice with whom it has been a pleasure to collaborate with throughout this project.

My gratitude also to Dr. Farid Boussaid whose offer to present this project at the 2009 PEECS seminar was a very valuable experience for me. Thanks also to all the staff and academics at the UWA Microelectronic Research Group.

More personally, I would like to thank my family and friends for all the support they have provided me over the last eight months: thank you for putting up with my busy-ness, running-around and rants!
# Table of Contents

1  INTRODUCTION ....................................................................................................................... 9  
1.1 Porous Silicon .......................................................................................................................... 10  
1.2 Overview of the Growth of Porous Silicon ............................................................................... 11  
1.3 Project Objectives .................................................................................................................... 14  

2  OPTICAL APPLICATIONS OF POROUS SILICON .................................................. 17  
2.1 Effective Medium Approximations .......................................................................................... 17  
2.2 DBRs and Fabry-Perot Filters .................................................................................................. 19  
   2.2.1 Effect of Refractive Index Contrast in DBRs .................................................................... 21  
2.3 Improving PS Fabrication for Optical Applications ............................................................... 22  
   2.3.1 Pulsed Anodisation .......................................................................................................... 23  

3  OPTICAL MODELLING ............................................................................................................ 25  
3.1 Thin Film Reflectance .............................................................................................................. 25  
3.2 Porosity Gradient Modelling ................................................................................................... 27  
3.3 Interface Roughness Modelling ............................................................................................... 28  
3.4 Front-End User Interface ......................................................................................................... 29  
   3.4.1 Structure Editor .............................................................................................................. 29  
   3.4.2 Porosity Gradient Modelling .......................................................................................... 31  
   3.4.3 Roughness Modelling .................................................................................................... 32  
3.5 Investigation Results ................................................................................................................. 32  
   3.5.1 Effect of DBR Period Count .......................................................................................... 32  
   3.5.2 Effect of FP Filter Porosity Gradients ............................................................................ 33  
   3.5.3 Effect of FP Filter Interface Roughness ......................................................................... 34  

4  PULSED CURRENT SOURCE .................................................................................................. 36  
4.1 Output Stage Investigation ...................................................................................................... 36  
   4.1.1 Experimental Results – Proof-of-Concept ...................................................................... 40  
   4.1.2 Error Amp Selection ........................................................................................................ 42  
   4.1.3 Heatsinking .................................................................................................................... 43  
   4.1.4 Safety and Failsafe Protection Systems ......................................................................... 44  
4.2 Digital to Analog Converter ................................................................................................... 45  
   4.2.1 Selection criteria/requirements ....................................................................................... 46  
   4.2.2 SPI Interface .................................................................................................................. 46  
4.3 Power Supply .......................................................................................................................... 47  
4.4 Complete Pulsed Current Source ........................................................................................... 48  
   4.4.1 Noise Reduction .............................................................................................................. 51  

5  MONITORING SYSTEMS ........................................................................................................ 52  
5.1 Analog to Digital Conversion .................................................................................................. 52  
   5.1.1 Part Selection .................................................................................................................. 52  
5.2 Signal Conditioning ................................................................................................................ 53  
   5.2.1 Common Mode Voltage Rejection .................................................................................. 53
1 Introduction

Porous silicon (PS) is a nano-material which consists of a silicon substrate into which pores are etched. The material exhibits optical and chemical properties which demonstrate potential for use in a diverse range of applications. These include optical filters such as Distributed Bragg Reflectors (DBRs) [1], chemical sensors [2] and point-to-point “fibre-optic” waveguide interconnects on integrated circuits [3]. A typical PS sample is shown below in Figure 1.1.

![Figure 1.1: A porous silicon sample (central coloured surface)](image)

High-performance reflectors such as DBRs find application in lasers [4] while the high surface-to-volume ratio of a PS structure allows the production of very sensitive chemical sensors. The ever increasing quest for digital computing power demands fast interconnects between on-chip components where on-die “fibre optics” may prove to be indispensable.

In order to best harness the characteristics of PS which make these applications possible, it is important to be able to control the precise formation of the PS structure. However current methods to produce PS often result in imperfections which adversely affect its performance in these applications.

This thesis will investigate these imperfections and attempt to devise a method for effectively controlling these imperfections. In particular, the high-quality production of multilayered PS structures for use in optical applications will be investigated. In addition, models will be developed to demonstrate the properties of PS and the effects of
anodisation imperfections. This will aid in better understanding the formation of PS and facilitate the effective use of PS in a wide range of applications.

1.1 Porous Silicon

Porous silicon is formed by the electrochemical anodisation of a silicon wafer in a hydrofluoric acid (HF) solution [5]. In this process, pores are etched into the silicon wafer which can vary from nanometres to microns in size, depending on the anodisation conditions. A cross-section of a typical multilayer PS structure of alternating porosity is shown in Figure 1.2.

![Figure 1.2: Cross-section of a porous silicon structure, from [6]](image)

Constructed from a silicon substrate, a PS layer (from here on synonymous with the term “film”) retains some of the properties of silicon. However with space in the structure for other substances to fill, the structure may behave like a composite material and take on some of the properties of the filling substance [6]. The proportion of the remaining silicon substrate left in a PS film in comparison to the original silicon substrate is referred to as the film's porosity, φ. This may be calculated as the remaining fractional volume of silicon as shown in Figure 1.3 or determined gravimetrically according to Equation (1.1).
**Introduction**

The porosity or fractional volume of a silicon substrate can be defined as:

\[ \phi = \frac{W_1 - W_2}{W_1 - W_3} \]  

where  
\( W_1 \) is the weight of the silicon wafer before anodisation  
\( W_2 \) is the weight of the wafer after anodisation  
\( W_3 \) is the weight of the wafer after the PS layer has been removed

It is this composite behaviour which is harnessed for the use of PS in optical applications. That is, crystalline silicon has a refractive index of around 3.5 [7], however when the pores in a PS film fill with air, then the refractive index of the resulting composite material has a refractive index between that of the upper bound set by silicon and that of the lower bound set by air (i.e \( n_{air} = 1 \)). Intuitively, the greater the proportion of air in the structure, the more it behaves like air, that is, it will have a lower refractive index.

**1.2 Overview of the Growth of Porous Silicon**

PS is produced by the anodisation of a silicon wafer in a hydrofluoric acid (HF) solution. The dissolution of silicon under anodisation is shown in the reaction described in *Equation (1.2)*. The production of a number of different by-products has implications for the uniformity of the anodisation process, discussed in *Chapter 2.3*.

\[ \text{Si} + 6\text{HF} \rightarrow \text{H}_2\text{SiF}_6 + \text{H}_2 + 2\text{H}^+ + 2e^- \]  

In order to perform the etching, an anodisation cell is used. A design which is currently being used at the University of Western Australia is shown in *Figure 1.4* and is shown schematically in *Figure 1.5*. The silicon wafer is mounted inside a Teflon anodisation cell which is submerged in the HF solution, with the Teflon material chosen due to its...
resistance to the highly corrosive properties of HF. Current is passed through the wafer via a conductive rubber back contact and a submerged platinum mesh electrode, again with the platinum material chosen due to its resistance to corrosion in HF.

Figure 1.4: Teflon PS anodisation cell in use at the University of Western Australia, courtesy [8]

Figure 1.5: Schematic view of the PS anodisation cell
Pérez [9] summarises the effect of HF concentration, anodisation current density, anodisation time, temperature and wafer doping on the porosity of the etched PS films. Controlling the HF concentration and the anodisation current density are the two common methods for controlling the porosity of films and their effects are summarised in Figure 1.6. However it was shown by Beale [10] that maximising of the range of porosities which can be produced cannot be achieved by controlling only one of these parameters alone. A reduced range of porosities directly limits the possible range of attainable refractive indexes – a key parameter used to design PS in optical applications. This relationship will be discussed in Chapter 2.1.

![Table: Effect on Produced Film](image)

<table>
<thead>
<tr>
<th>Increased Parameter</th>
<th>Porosity</th>
<th>Etch Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>HF Concentration</td>
<td>decrease</td>
<td>decrease</td>
</tr>
<tr>
<td>Current Density</td>
<td>increase</td>
<td>increase</td>
</tr>
</tbody>
</table>

*Figure 1.6: Effect of HF concentration and current density on produced films*

Various optical devices such as DBRs and Fabry-Pérot filters require multilayered structures of differing properties to be constructed. To this end, Pavesi [1] describes a process where it is possible to fabricate multilayered PS films suitable for these applications by periodically varying the anodisation current density throughout an etch process. This produces a PS film with certain properties (*Figure 1.7a*) and then another PS film below the first with different properties (*Figure 1.7b*). The production of a film layer depletes the carrier population on the pore surface, preventing further etching of the pore wall. As a consequence, etching proceeds primarily at the pore tips, resulting in etching which is highly directional. This also means that films which have already been formed are minimally affected by further etching under the same or different conditions.
1.3 Project Objectives

It was shown that porosity of a PS film is strongly dependent on the anodisation current density and HF concentration [1, 9]. It was also shown that non-uniformities such as interface roughness and porosity gradient can be controlled and minimised using pulsed current anodisation [11, 12] and low temperatures [3, 13] during anodisation. Specifically, it is important to reduce the magnitude of both of these parameters in order to achieve the highest performance in terms of stop-band width and peak stop-band reflectivity. This is modelled in Chapter 2.2.

To overcome these issues, a system has been proposed which would facilitate the control of etch parameters in an effort to control porosity, porosity gradient and interface roughness. This would afford users the ability to set parameters which would offer low interface roughness and porosity gradient whilst maximising the range of PS porosities, and thus refractive indexes. The result is the opportunity to produce high-performance and high-quality optical devices, such as DBRs, from PS.

The system block diagram shown in Figure 1.8 can be broken down into 3 sections which are highlighted in the figure:

1. Pulsed current supply
2. Monitoring and logging system
3. A gantry
The pulsed current supply would provide control over the anodisation current amplitude, frequency and duty cycle. It is desired that the pulse frequency can be programmed up to 10 kHz with a minimum pulse duration of 10 µs (i.e. 10% duty cycle). In consideration of the minimum pulse length, a rise time of 1 µs is desired. Current amplitude should be controllable in 1 mA increments from 1 mA to 1.5 A, providing a current density of up to around 150 mA/cm² for a 35 mm diameter wafer. A voltage limit of 20 V should also be available, equivalent to the voltage specification of the Agilent supply currently used in PS studies at the University of Western Australia.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Desired</th>
<th>Agilent 6612C</th>
<th>Keithley 220</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current</td>
<td>1.5 A</td>
<td>2.0 A</td>
<td>±101 mA</td>
<td>(max.)</td>
</tr>
<tr>
<td>Output voltage</td>
<td>20 V</td>
<td>20 V</td>
<td>105 V</td>
<td>(max.)</td>
</tr>
<tr>
<td>Response time</td>
<td>1 µs</td>
<td>&lt;100 µs</td>
<td>&lt;3 ms</td>
<td>to 1%/99%</td>
</tr>
<tr>
<td>Accuracy</td>
<td>1 mA</td>
<td>0.5 mA</td>
<td>0.1 mA</td>
<td>at full load</td>
</tr>
</tbody>
</table>

A comparison of the desired specifications to those of the Agilent 6612C and Keithley 220 supplies used at the University of Western Australia is shown in Figure 1.9. Of significant interest is the desired response time (output current waveform rise and fall time). If successful, the supply will have a response time two orders of magnitude better.
than the currently used commercial Agilent unit. This will provide researchers at The University of Western Australia with a unique tool to investigate PS.

The monitoring system samples the PS I-V characteristics throughout an etch process. This will aid in gaining a better understanding into the formation of PS. The system should offer I-V characterisation with precision to 1 mV and 1 mA, reflecting the desired programming current resolution of the pulsed current supply.

The gantry is being designed and constructed by another final year student at The University of Western Australia, also under the supervision of Dr. Adrian Keating, which will be used to move the PS sample between different electrolytes baths with different HF concentrations.
2 Optical Applications of Porous Silicon

PS shows potential for use in optical applications as the small size of the pores means that the PS structure acts as a uniform composite of silicon and air. This means that the structure has an effective refractive index which exists somewhere between that of silicon and air.

Optical applications for PS such as DBRs, Fabry-Pérot and other optical filters make use of the interference effects which occur due to reflections at the interface between bodies of differing refractive index. Through the effects of constructive and destructive interference it is possible to tune the reflective properties of an optical filter formed using PS.

2.1 Effective Medium Approximations

In order to quantify the relationship between porosity and effective refractive index, effective medium approximations (EMAs) are used which attempt to model non-homogeneous materials as homogeneous materials with equivalent properties. Some EMAs and the relationship they describe in terms of dielectric permittivity include:

- The Maxwell-Garnett Theory (MGT) [16]:

  \[ \varepsilon_{\text{eff}} = \varepsilon_{r,c} \left( 1 - \frac{3\phi(\varepsilon_{r,c} - \varepsilon_{r,d})}{\varepsilon_{r,d} + 2\varepsilon_{r,c} - \phi(\varepsilon_{r,c} - \varepsilon_{r,d})} \right) \]

- The Bruggeman model [7]:

  \[ \varepsilon_{\text{eff}}^3 - 3\varepsilon_{r,d}\varepsilon_{\text{eff}}^2 + \left( 3\varepsilon_{r,d}^2 - (1 - \phi)^3 \left( \frac{1}{\varepsilon_{r,c}} \right) (\varepsilon_{r,c} - \varepsilon_{r,d})^3 \right) \varepsilon_{\text{eff}} - \varepsilon_{r,d}^3 = 0 \]

- The volume averaging theory (VAT) which was combined with Maxwell’s equations by del Rio in [17]:

  \[ \varepsilon_{\text{eff}} = (1 - \phi)\varepsilon_{r,c} + \phi\varepsilon_{r,d} \]

where \( \varepsilon_{\text{eff}} \) is the real dielectric permittivity of the effective medium

\( \varepsilon_{r,d} = n_{r,d}^2 \) is the real dielectric permittivity of the pore spaces (i.e. air for PS)

\( \varepsilon_{r,c} = n_{r,c}^2 \) is the real dielectric permittivity of the substrate (i.e. silicon for PS)

\( \phi \) is the porosity of the film (ratio of pore spaces to substrate)
These EMAs, as well as others, are covered by Braun et al. in [7] where the conditions under which these EMAs can be applied are discussed. They concluded that most models usually provided “acceptable predictions” to the relationship between film porosity and refractive index. However, it was noted that the VAT based model provided superior approximations to the relationship which exists when the two materials in the structure have quite dissimilar refractive indexes, such as in the case of PS in optical applications where the refractive index contrast ratio between silicon and air is greater than 3:1 ($n_{Si}: n_{air}$).

A comparison between the MGT, Bruggeman and VAT model are shown in Figure 2.1.

![Porous film refractive index using EMAs](image)

**Figure 2.1: Comparison of the MGT, Bruggeman and VAT EMAs**

Although differing in the predicted refractive index, they indicate a similar general relationship and as such, regardless of the particular EMA used, it can be seen that there is a strong (almost linear) relationship between the porosity of a film and the expected refractive index that results.
2.2 DBRs and Fabry-Perot Filters

Two possible applications for PS are Distributed Bragg Reflectors (DBRs) and Fabry-Pérot Filters. Wave reflections occur at each PS film interface due to the refractive index changes. This is shown in Equation (2.1) and can be simplified to Equation (2.2) at optical frequencies where $\mu_r = 1$ with normal incidence to the film. With each layer separated spatially, the reflected waves recombine through constructive and destructive interference with a phase difference to that of the incident wave.

$$R = \frac{E_r}{E_i} = \frac{(n_2/\mu_2) \cos \theta_i - (n_1/\mu_1) \cos \theta_t}{(n_2/\mu_2) \cos \theta_i + (n_1/\mu_1) \cos \theta_t}$$  \hspace{1cm} (2.1)

$$R_{\text{normal}} = \frac{n_2 - n_1}{n_2 + n_1}$$  \hspace{1cm} (2.2)

A DBR consists of layers of material with alternating high and low refractive indexes with each layer selected to be a quarter-wavelength of a target wavelength, shown in Figure 2.2a. In this configuration, within the “passband” region of the reflectance spectra, the interference of all reflected waves combine at the top surface of the DBR in phase, resulting in constructive interference and thus high reflectivity.

![Figure 2.2: Schematic cross-section of a DBR and Fabry-Pérot Filter](image)

Figure 2.3 shows the effect of having more periods in the DBR or by using a higher contrast ratio between the refractive index of the high and low refractive index layers.
With more periods and/or higher contrast ratio, the width of the high-reflectivity stop-band plateau is higher in magnitude, has a sharper stop-band edge and is wider.

Fabry-Pérot Filters are basically two DBRs separated by a $\lambda/2$ thickness spacer layer, shown in Figure 2.2b. In this case, resonance occurs at integer multiples of twice the thickness of the space layer resulting in an optical filter which transmits only a small range of wavelengths while others are reflected [1].

Figure 2.4 shows the effect of using a higher contrast ratio between the refractive index of the high and low refractive index layers. With a higher contrast ratio, the width of the low-reflectance pass-band is much sharper. A similar effect can be observed when using more periods in the DBRs which surround the half-wavelength Fabry-Pérot cavity.

![DBR Reflectance Spectrum](image)

*Figure 2.3: Effect of periods and refractive index contrast ratio on DBR reflectivity*
2.2.1 Effect of Refractive Index Contrast in DBRs

The reflectance, $R$, of a DBR and its dependence on the refractive indexes of the layers which make up the DBR can be described using the following equation for the reflectance of multilayer dielectric coatings [18]:

$$ R = \left( \frac{1 - (n_H/n_L)^{2p} (n_H^2/n_S)^2}{1 + (n_H/n_L)^{2p} (n_H^2/n_S)^2} \right)^2 $$  \hspace{1cm} (2.3)

where
- $n_H$ is the refractive index of the high-index layer
- $n_L$ is the refractive index of the low-index layer
- $n_S$ is the refractive index of the medium on the transmitted side
- $2p + 1$ is the number of layers in the stack

*Figure 2.4: Effect of refractive index contrast ratio on Fabry-Pérot filter reflectivity*
Figure 2.5 plots Equation (2.3) over a range of refractive indexes, as well as number of film layers. It shows that the contrast in refractive indexes, $n_H/n_L$, plays an important role in the DBR’s reflectivity, especially when only a few layers are used. Thus, maximisation of $n_H/n_L$ greatly increases the optical performance of DBRs.

From the discussion on EMAs in Chapter 2.1, this can be achieved by attaining the maximum possible modulation of PS porosities. As discussed in Chapter 1.2, this can be made possible through control of HF concentration and current density. These capabilities are made available through the use of a gantry (to provide access to multiple HF bath concentrations) and a controllable current source, as discussed in Chapter 1.3.

2.3 Improving PS Fabrication for Optical Applications

During the anodisation of silicon, conditions within a growing pore change: the HF concentration decreases and $H_2$ bubbles are produced on the PS surfaces [19]. A lack of equilibrium, as demonstrated by Xu et al. [20], has shown the changes which occur in the I-V characteristics during anodisation. The decrease in the HF concentration, depletion in the number of available holes on the pore walls and the production of $H_2$ adversely
affects the etching of the crystalline silicon and changes the etching parameters indicated by changes in the properties of films produced by subsequent etching. This represents unpredictable and irregular deviations from the expected “ideal” etching process and thus differences between the films produced and those which were expected. The resulting non-uniform anodisation affects the porosity of the layers (a porosity gradient) and creates irregular surfaces between layers of differing porosities (interface roughness). Both of these factors are detrimental to the performance of optical filters which may be produced from PS.

2.3.1 Pulsed Anodisation

Inspired by several methods suggested by Bomchil et al. [11] to remove hydrogen bubbles, several studies by Xiong et al. [12] have demonstrated improvements in film quality when using pulsed current anodisation as opposed to DC anodisation. Comparisons between the two anodisation methods [12] make note of more uniform pore distributions and flatter surfaces for PS samples produced using pulsed anodisation. Studies at The University of Western Australia by James et al. [21] have studied the effects of pulsed anodisation frequency and duty cycle on the properties of PS films in terms of interface roughness and porosity gradient. Their results showed significant reductions in interface roughness and porosity gradient when using a low-frequency pulsed current source as opposed to using a DC anodisation source. These results are shown in Figure 2.6 and Figure 2.7 which show that current pulse frequencies below around 1 Hz with duty cycles less than 15% resulted in porosity gradients which dramatically reduce to almost zero and similar current characteristics providing interfaces with no measurable interface roughness.
Figure 2.6: Effect of pulsed current anodisation on interface roughness, from [21]

Figure 2.7: Effect of pulsed current anodisation on porosity gradient, from [21]
3 Optical Modelling

As discussed in Chapter 2.3, fabrication of porous silicon may result in porosity gradients and interface roughness. This section of the project attempts to provide models which allow investigation into the effects of porosity gradient and interface roughness in terms of their effect upon the performance of optical devices fabricated from porous silicon.

3.1 Thin Film Reflectance

In a single dimension, the reflectance of a thin film can be described in terms of the electric, $E$, and magnetic, $H$, components of the electromagnetic fields at the film boundaries [18]. This is shown in Equations (3.1) and (3.2).

$$E_a = E_b \cos \delta + H_b \frac{i \sin \delta}{\eta}$$  \hspace{1cm} (3.1)

$$H_a = E_b i \eta \sin \delta + H_b \cos \delta$$  \hspace{1cm} (3.2)

where $E_a$ and $H_a$ are the electric and magnetic fields at the incident face

$E_b$ and $H_b$ are the electric and magnetic fields at the transmittance face

$\delta$ is the wave phase change through the film layer

$\eta$ is the layer optical admittance

The parameter $\delta$ in Equations (3.1) and (3.2) represents the change in phase of the wave between the two sides of the film and is dependent upon the film’s refractive index, $n$, the film thickness, $d$, the angle of incidence and the incident wavelength, $\lambda$. In the case of normal incidence, the expression for $\delta$ is shown in Equation (3.3).

$$\delta = \frac{2\pi nd}{\lambda}$$  \hspace{1cm} (3.3)

Equations (3.1) and (3.2) can be represented in matrix form as shown in Equation (3.4).

$$\begin{bmatrix} E_a \\ H_a \end{bmatrix} = \begin{bmatrix} \cos \delta & \frac{i \sin \delta}{\eta} \\ i \eta \sin \delta & \cos \delta \end{bmatrix} \begin{bmatrix} E_b \\ H_b \end{bmatrix}$$  \hspace{1cm} (3.4)

This equation can be used to define the film’s characteristic matrix which is useful when attempting to determine the optical properties of multilayered films. The characteristic matrix component of Equation (3.4) is shown in Equation (3.5).
\[ M = \begin{bmatrix} \cos \delta & i \sin \delta \\ i \eta_1 \sin \delta & \cos \delta \end{bmatrix} \]  

(3.5)

In order to determine the effective characteristic matrix of an assembly of thin films, such as occurs when creating multilayered structures, it is only necessary to pre-multiply the characteristic matrix of each layer with the layer which exists on the former’s transmittance side. That is, for a two layered structure with the first layer, L1, being the incident layer, then the system’s characteristic matrix is given by:

\[ M_{sys} = \begin{bmatrix} \cos \delta_2 & i \sin \delta_2 \\ i \eta_2 \sin \delta_2 & \cos \delta_2 \end{bmatrix} \begin{bmatrix} \cos \delta_1 & i \sin \delta_1 \\ i \eta_1 \sin \delta_1 & \cos \delta_1 \end{bmatrix} \]  

(3.6)

In the general case for a structure with \( k \) film layers, the expression for the system’s characteristic matrix is shown in Equation (3.7) for the correct order of the individual matrices’ multiplication. The equivalent expression for a thin film assembly to Equation (3.4) is shown in Equation (3.8).

\[ M_{sys} = \prod_{y=1}^{k} \begin{bmatrix} \cos \delta_y & i \sin \delta_y \\ i \eta_y \sin \delta_y & \cos \delta_y \end{bmatrix} \]  

(3.7)

\[ \begin{bmatrix} E_a \\ H_a \end{bmatrix} = M_{sys} \begin{bmatrix} E_b \\ H_b \end{bmatrix} \]  

(3.8)

To determine the assembly’s reflectance, we must first determine the system admittance according to Equation (3.9).

\[ Y = \frac{1}{Z_0} \frac{E_a}{H_a} \]  

(3.9)

where \( Z_0 \) is the impedance of free space, \( \frac{1}{\epsilon_0 c_0} \approx 376.7 \ \Omega \)

Using this parameter, we can then determine the system reflectance using (3.10).

\[ R = \left( \frac{Y_0 - Y_1}{Y_0 + Y_1} \right) \left( \frac{Y_0 - Y_1}{Y_0 + Y_1} \right)^* \]  

(3.10)

It is this expression which is used in the PS modelling program to determine the reflectance spectra of a multilayered PS structure.
3.2 Porosity Gradient Modelling

To model a porosity gradient, the method previously used at the University of Western Australia was used. Specifically, this method aims to model a gradual change in porosity throughout the depth of a film as a series of small, discrete steps.

Due to the quantisation of the gradient, it is important to provide a sufficient number of steps so as to best represent the gradual nature of the porosity change. Splitting the gradient into 32 steps has been suggested to be effective [21] and is used in the PSAnalysis program, although the MATLAB script supports a variable number of steps which can be specified at runtime through the use of a function input parameter. A sample of this code is shown in Figure 3.1.

Using the original matrix which describes the structure (denoted as matprop), a new layer matrix is produced (denoted as matproplayer). To this matrix, an incremental porosity is added (pergrad) and the incremental layer thickness specified. Note that in this case, the pergrad value is a pre-calculated constant throughout the loop. This means that a linear porosity gradient is applied to the structure. It is possible to create a non-linear porosity gradient by changing the pergrad variable into a matrix and pre-loading it with a non-linear normalising function. This layer matrix is then appended onto a new structure matrix which represents the system modelled with a porosity gradient. The result is a matrix which describes a structure with many times more layers than the original, but with a constant refractive index in each layer.

```matlab
for j=0:slices-1
    % Add incremental porosity to the new “sub-slice” layer
    matproplayer(1) = matprop(i+1,1) * (1 + (i*slices + j)*pergrad);

    % Set layer thickness for this “sub-slice”
    matproplayer(2) = matprop(i+1,2)/slices;

    % Add this “sub-slice” to the overall structure
    matpropstruct = cat(1, matpropstruct, matproplayer);
end
```

*Figure 3.1: Simplified MATLAB implementation of porosity gradient modelling*
3.3 Interface Roughness Modelling

The Bennet-Davies method [22] is used to model the effects of interface roughness on the performance of PS optical filters. The relationship is shown in Equation (3.11) and relates the RMS roughness of the surfaces, the incident wavelength and the reflectance of the structure neglecting roughness to the reflectance of the structure including roughness.

\[
R = R_0 \exp\left( -\left(\frac{4\pi\sigma}{\lambda}\right)^2 \right)
\]  

(3.11)

where \( R_0 \) is the structure reflectivity according to Equation (3.10)

\( \sigma \) is the RMS interface roughness

\( \lambda \) is the incident wavelength

This relationship is implemented as the last step of the reflectance calculation using the reflectance calculated using the matrix method, described in Equation (3.10). A sample of the code which is used in the MATLAB model is shown in Figure 3.3.

```matlab
% Standard reflection calculation according to Fresnel's equations
reflectance(n) = reflect_s(matpropstruct,wavelengths(n));

% Compensation for roughness
reflectance(n) = reflectance(n)*exp(-((4*pi*roughness/wavelen(n))^2));
```

Figure 3.3: MATLAB extract showing application of roughness parameter to reflectance
3.4 Front-End User Interface
To enhance the user experience to the modelling tools which were developed, a front-end graphical user interface (GUI) was developed using Microsoft Visual Studio tools, specifically Microsoft Visual Basic 2008. This development environment was chosen due to the author’s background in its use and it was felt that it would provide a cleaner and easy-to-use interface.

The program, called PSAnalysis, provides users with the ability to use the MATLAB programs developed whilst never having to deal with the MATLAB command line. This also lessens the required learning curve to utilise the modelling tools as users do not need to learn the details of how to operate the MATLAB functions (such as the parameters which need to be passed).

3.4.1 Structure Editor
The GUI allows users to configure any multilayer, one-dimensional optical structure by specifying the following parameters for each layer:

- Layer thickness (Depth)
- Refractive index or porosity

When entering a porosity parameter, users can select from one of three effective medium approximations (as discussed in Chapter 2.1) which is used to convert the specified layer porosities into refractive indexes which are used by the modelling program.

*Figure 3.4a shows the Layer Editor tab which is the most primitive form of input for the program. This tab is also used to edit layer properties which have already been specified in the structure.*
Figure 3.4: The “Layer Editor” tab allows configuration and editing of structures while design of DBR and FP filters is supported through the DBR/FP Analysis tab

In order to expedite simulation of common multilayer optical structures, the DBR/FP Analysis tab allows for the quick addition of a DBR or FP filter structures. This tab is shown in Figure 3.4b. Users can specify the refractive indexes of the layers used in the structure, as well as the desired centre wavelength (that is, the centre wavelength of a DBR’s stopband or the wavelength of a FP filter’s passband) and the thickness of the silicon substrate which exists after the filter’s layers.

As new layers and structures are added using the DBR/FP Analysis tab or the Layer Editor tab, they are recorded in the Structure Viewer, shown on the left in Figure 3.5. To aid in visualising the structures which are listed in the Structure Viewer, a simple cross-sectional view of the structure is provided, shown on the right in Figure 3.5. The graphical display window supports simple panning and zooming functions.
3.4.2 Porosity Gradient Modelling

The PSAnalysis program also allows modelling of the effects of porosity gradients. This tool is accessed from the Structures tab and is shown in Figure 3.6a. The severity of the gradient can be specified in terms of an absolute change (for example, a change from an ideal (specified) refractive index of $n=2.0$ in the structure editor to $n=2.5$ is input into the program as a value of 0.5) or as a percentage of the ideal (specified) refractive index. Gradients are applied proportionally across the entire structure, not across the individual layers. The effects of porosity gradients can therefore be investigated by specifying two identical structures but applying a different porosity gradient parameter to each.

Also visible in Figure 3.6a, is the option to select a gradient characteristic. Due to limitations in the current MATLAB program which is used in the background, only a linear gradient is currently supported, however additional gradient characteristics can be added with suitable modifications to the underlying MATLAB program.
3.4.3 Roughness Modelling

A facility is provided in the PSAnalysis program to model the effects of interface roughness. This tool is accessed from the Structures tab and is shown in Figure 3.6b. It supports the application of a single RMS roughness value to a structure which is specified in nanometres. Although only one roughness value can be applied for each individual structure, a different roughness value can be applied to each structure. The effects of interface roughness can therefore be investigated by specifying two identical structures but applying a different interface roughness parameter to each.

3.5 Investigation Results

Three tests will be discussed to demonstrate the insight the PSAnalysis program can quickly provide users with regards to:

1. The effects of the number of periods on DBR reflectivity
2. The effects of porosity gradients on the FP filter reflectance spectrum
3. The effects of interface roughness on the FP filter reflectance spectrum

3.5.1 Effect of DBR Period Count

From the discussion in Chapter 2.2.1, Equation (2.3) suggests that an increase in the number of periods in a DBR will result in an increase in the reflectivity of the DBR structure. To test this, three DBR structures ranging from three to five periods were configured in PSAnalysis with a design centre wavelength of 600 nm and layers with refractive indexes of n=1.5 and n=2.5.

The output plot produced by the PSAnalysis program is shown in Figure 3.7. The result follows our expectation based upon Equation (2.3) with an increase in peak reflectivity from around 94% using a DBR with 3 periods to around 99% using a DBR with 5
periods. Furthermore, it is also possible to notice a sharpening in the transition period between the passband and stopband regions of the reflectivity spectrum plot.

![Reflectivity spectrum plot](image)

**Figure 3.7: Effect of the number of periods in a DBR**

### 3.5.2 Effect of FP Filter Porosity Gradients

As discussed in Chapter 2.1, the porosity of a PS film is related to the refractive index of that film layer. Furthermore, in Chapter 2.2, it is discussed that the thickness of the central spacer layer is a function of the layer’s refractive index and the desired centre passband wavelength of the FP filter. It follows that if there are any unexpected deviations in the refractive indexes of the PS layers (such as occurs when porosity gradients occur) then the refractive index of the layer will change and thus the expected centre wavelength is no longer valid – there will be a shift in the passband wavelength.

To test this theory, three FP structures with three periods and linear porosity gradients of varying magnitude from 0% (no gradient) to 20% were configured in the *PSAnalysis* program with a design centre passband wavelength of 600 nm and layers with refractive indexes of n=1.5 and n=2.5.
The output plot produced by the PSAnalysis program is shown in Figure 3.8. The plot confirms our expectations with a shift in the passband wavelength from the design wavelength of 600 nm to around 540 nm when a gradient of 20% exists. The plot also reveals a narrowing of the filter’s stopband range and a decrease in the filter’s transmittance outside the stopband region.

![Figure 3.8: Effect of porosity gradients in a FP filter](image)

### 3.5.3 Effect of FP Filter Interface Roughness

Intuitively, interface roughness in an optical filter can be considered to be equivalent to attempts to get a reflection from a mirror with a sandpapered surface. In light of this line of thought, we can expect that an optical filter with interface roughness will result in poor reflectivity properties in comparison to a filter which has less (or no) interface roughness.

To test our intuition, three FP structures with three periods and RMS interface roughness values ranging from 0 nm (no roughness) to 20 nm were configured in the PSAnalysis program with a design centre passband wavelength of 600 nm and layers with refractive indexes of n=1.5 and n=2.5.
The output plot produced by the *PSAnalysis* program is shown in *Figure 3.9*. The plot reflects our expectations with significant degradation in the high reflectivity passband reflectivity from a peak of around 98% with no roughness to around 86% when there is an RMS roughness of 20 nm.

![Figure 3.9: Effect of roughness in a FP filter](image)

The plot also reveals that the effects of interface roughness are more pronounced (that is, there is even less attenuation in the stopband) for shorter wavelengths. This can be attributed to a fixed roughness parameter and the fact that shorter wavelengths experience greater scattering than longer wavelengths. It also shows a slight widening of the passband spectrum. This corresponds to the suggestion that scattering results in an increase in transmittance outside the passband [23].
4 Pulsed Current Source

This project aims to design, construct and test a self-contained supply which can compete with the advertised performance specifications of the Agilent 6612C power supply which is currently used in PS studies at the University of Western Australia. However, unlike the Agilent 6612C, the unit would also be required to control switching properties and produce arbitrary current waveforms. The supply should cater for pulsed currents at a range of frequencies from 0.1 Hz to 10 kHz and an adjustable duty cycle from 10% to 90%. Capability should also be provided to provide DC anodisation (constant current). This criteria provides the capability to reproduce the 1 kHz experiments demonstrated by James et al. [21], while allowing the opportunity to explore the effects of even higher frequencies where previous experimental results, shown in Figure 2.6, suggest that RMS roughness increases dramatically. It is aimed that the supply’s switching characteristics have a transient period less than 10% of the on time and overshoot no more than 10% of the programmed current level. Some of these specifications are shown in Figure 4.1.

![Figure 4.1: Desired output waveform specification limits](image)

4.1 Output Stage Investigation

Tests were run using two prototyped constant current supplies: the first based on the readily-available 7805/LM317 voltage regulators and the second based on a discrete design. The integrated design utilises designs in the devices’ datasheets [24, 25] while the discrete design is shown in Figure 4.3.
The design shown in Figure 4.3 depicts a current shunt design which modulates the voltage at the gate of the pass MOSFET, Q1, which in turn controls the current through the load, R1. Current amplitude is controlled using variable resistor VR2 in the feedback path. The reference voltage provides rejection of power supply fluctuations and can be adjusted using VR1. In addition to the original regulator design, Figure 4.3 also shows the circuit used to provide current pulsations: digital switching pulses are provided via the PWM signal line which produces current pulses by controlling Q3 and Q4.

Results for output current ripple into a 3.65 Ω resistive load (and oscilloscope with 25 pF||1 MΩ input) with no switching is summarised in the table in Figure 4.2.

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Design</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7805</td>
<td>0.46A (0.46A)</td>
</tr>
<tr>
<td></td>
<td>LM317</td>
<td>0.11A (0.22A)</td>
</tr>
<tr>
<td></td>
<td>LM317</td>
<td>0.27 (0.27)</td>
</tr>
<tr>
<td></td>
<td>Discrete</td>
<td>0.35A (Note 1)</td>
</tr>
<tr>
<td>V_s = 12V</td>
<td>1.37</td>
<td></td>
</tr>
<tr>
<td>V_s = 12-16V (≈2Hz)</td>
<td>2.74</td>
<td>2.74</td>
</tr>
</tbody>
</table>

Note 1: Below measurable limits of oscilloscope used for tests

Figure 4.2: Desired output waveform specification limits

Figure 4.3: Initial discrete current regulator with load switching

The 7805/LM317 designs were discarded as they exhibited relatively high levels of noise. As a result, pulsation experiments to analyse its transient response were only performed on the discrete regulator design. Although 2048, 4096 and 8192 Hz switching frequencies
yielded inconclusive results with the oscilloscope used, the test revealed high power dissipation in the shunt. This resulted in some design modifications to the feedback systems including the use of an operational amplifier which allows the use of a smaller current sense resistor.

The current control scheme suffered significant switching overshoot because the switching system was independent from the feedback system. When the switching system disconnects the load, the regulator tries to maintain the output current by turning the FET hard on. However, as soon as the load is reconnected, the system takes time to lower the current back down which results in large overshoot, especially at low output currents.

The solution was to redesign the system by making the switching system part of the feedback system – operating the system much alike an error amp in a typical voltage regulator. This method would also facilitate the generation of arbitrary current waveform shapes as opposed to simply “on-off”. A block diagram of this scheme is shown in Figure 4.4 and the output stage of the supply is shown in Figure 4.5.
The output stage transistor emitter current can be calculated to be as shown in Equation (4.1).

\[
I_E = \frac{RI_L + G(R + R_S)(V_{in} + V_{io}) - G R_S (R I_L - V_{BE}) - V_{BE}}{R + R_S}
\]  
(4.1)

where \( R_S \) is the current sense resistance
\( R \) is the drive transistor base resistance
\( G \) is the opamp open-loop gain
\( V_{in} \) is the non-inverting opamp voltage
\( V_{io} \) is the opamp input offset voltage

With a typical open-loop gain in the order of 100 dB, Equation (4.1) approximates to that shown in Equation (4.2).

\[
I_E = \frac{V_{in} - V_{io}}{R_S}
\]  
(4.2)

This gives a transistor collector current, which is equal to the load current, as shown in Equation (4.3).

\[
I_C = \frac{\beta}{\beta + 1}I_E
\]
\[
I_C = \alpha \frac{V_{in} - V_{io}}{R_S}
\]  
(4.3)
where $\beta$ is the transistor current gain

\[
\alpha = \frac{\beta}{\beta + 1} \approx 1 \text{ for large } \beta
\]

Thus, with selection of an operation amplifier with a very small input offset voltage, we find a transconductance relationship:

\[
I_C \propto V_{in}
\]  \hspace{1cm} (4.4)

Figure 4.6 shows the error in the ideal system transconductance of 1 A/V when using a 1 $\Omega$ current sense resistor and assuming a transistor gain, $\beta = 60$ and $V_{BE} = 0.92$ V. With a linear current error, it should be quite trivial to correct the error through software compensation for currents above a few milliamps.

4.1.1 Experimental Results – Proof-of-Concept

Tests were conducted to test the effectiveness and capabilities of the proposed current source output stage into a 1 $\Omega$ load using a TIP41C output transistor, a 1 $\Omega$ current sense resistor and an LM358 operational amplifier. Except for the use of a higher performance operation amplifier, this setup is the same as that which was used in the final circuit.
design. Also, in place of a DAC, an Agilent 33220A function generator was used for these proof-of-concept experiments.

Current measurements were obtained by measuring the voltage across the current sense resistor. As shown in Equation (4.3), the voltage measured across this resistor is proportional to the current through it and is approximately equal to the current through the load resistor (minus the output transistor base current, which is at least an order of magnitude smaller due to the TIP41C’s current gain, $\beta$).

*Figure 4.7* shows the function generator configured to provide a 100 mV square wave at a frequency of 10 kHz. With a system transconductance of 1 A/V, we should expect an output current of 100 mA. The resultant voltage across the current sense resistor is shown to have an amplitude of approximately 100 mV. This suggests a current through the load of around 100 mA, as expected. A small amount of overshoot can also be observed on the pulse edges, particularly on the rising edge.

*Figure 4.7: Input reference on top trace with voltage across 1Ω current sense resistor on bottom trace, producing 100 mA square wave at 10 kHz*

*Figure 4.8* demonstrates the system’s ability for the output current to be controlled. By changing the function generator’s output to provide pulses with an amplitude of 500 mV, a 500 mA current can be seen to flow. The presence of overshoot can be seen clearly in *Figure 4.8* and can be attributed to the slow speed of the LM358 operational amplifier which was used in these tests. As shown in *Chapter 4.4*, the use of a high speed operational amplifier helps to reduce the overshoot which the system experiences.
4.1.2 Error Amp Selection

As suggested in Equations (4.1), (4.2) and (4.3), sources of system error may arise due to factors such as:

- Operational amplifier input offset voltage
- Operational amplifier gain
That is, to reduce output error, an operational amplifier chosen for use as the system’s error amplifier should have low input offset voltage and a high gain. With a typical input offset voltage of 150 μV and an open-loop gain of greater than 100 dB [26], the Texas Instruments OPA350 series of operational amplifiers was selected for this application.

### 4.1.3 Heatsinking

In order to reduce noise on the output of the supply, the system adopts a linear system as opposed to a switching system. This comes at the cost of potentially low system efficiency and this leads to high system power dissipation. In fact, the system can be quite easily be related to a Class A audio amplifier with a dynamically controllable quiescent current. This power is primarily dissipated across the output drive stage transistor (shown as Q1 in Figure 4.5).

With a supply voltage of 25 V and a maximum load current of 1.5 A using a 1 Ω current sense resistor and considering that the maximum voltage across the transistor, $V_{CE}$, will occur during a short circuit load condition (that is, $V_{load} = 0$ V), then the voltage across the transistor is:

$$V_{CE} = V_s - R_s I_E$$
$$\approx V_s - R_s I_L$$
$$= 25 V - 1.5 V$$
$$= 23.5 V$$

The power dissipation is therefore:

$$P_D \approx V_{CE} I_E$$
$$= 23.5 V \times 1.5 A$$
$$= 35.25 W$$

The maximum allowable junction temperature of the TIP41C transistor device is 150°C [27], however to provide a degree of safety margin, as well as to provide additional system stability and reduce system thermal stresses, a maximum thermal design junction temperature of 140°C was selected. With an externally mounted heatsink and for use in an indoor and air-condition controlled environment, a maximum ambient temperature
of 30°C was selected. The maximum allowed total thermal resistance from junction to ambient, $R_{th(j-a)}$ is therefore:

$$R_{th(j-a)} = \frac{T_j - T_a}{P_D} = \frac{140 - 30}{35.25} = 3.121 \, ^\circ C/W$$

The required heatsink thermal resistance is given by [28]:

$$R_{th(hs)} = R_{th(j-a)} - R_{th(j-c)} - R_{th(c-hs)} = 3.121 - 1.67 - 0.8 = 0.651 \, ^\circ C/W$$

A 200 mm channel type heatsink was selected with a quoted thermal resistance of 0.75 °C/W [29]. Although this is higher than the calculated required thermal resistance, it was chosen for several reasons:

- The power dissipation used in the calculation is a worst case scenario and is significantly higher than that which would be experienced under normal usage scenarios
- Additional heat dissipation capability can be provided by attaching a fan onto the heatsink, thus providing better power handing capabilities whilst reducing cost and size

### 4.1.4 Safety and Failsafe Protection Systems

The system provides two protection methods to protect the system, external equipment and the user from fault conditions.

Short circuit conditions are the most likely source of failure with a short circuit of the primary supply (+25 V) to ground being of major concern, second only to failure of the 240 V mains powered sections. In any case, both of these systems (the 25 V circuit supply and 240 V transformer supply) are individually fused.

In the event of controller failure, mechanical relay switches are included in-line with the output supply which can physically break the output connection. The driver systems for
these relays are also configured to fail-safe: the normal position for these relays is in the open position which isolates the output from the supply.

### 4.2 Digital to Analog Converter

In order to produce a reference voltage to set the desired current level for the constant current source, a digital to analog converter (DAC) was used. A DAC accepts a digitally programmed number and produces a voltage which is proportional to this digital representation, usually as some proportion of an internally generated or externally supplied reference voltage.

There are many different criteria which may be used to decide the appropriateness of a DAC of a particular application. Four specifications are of particular significance to the use of a DAC in the application of a DAC to the current source supply.

1. **Resolution**
   
The DAC resolution determines the size of the output voltage step for a unit increase in the programmed value in the DAC. A 10-bit DAC provides $2^{10} = 1024$ voltage steps whereas a 12-bit DAC can provide $2^{12} = 4096$ voltage steps. The size of each step for a unipolar (only positive or negative voltages) DAC output can be found using Equation (4.5).

   $$\Delta V = \frac{V_{ref}}{2^n} \quad (4.5)$$

2. **Sample rate**
   
The sample rate defines the maximum rate at which the DAC can accept a new data value.

3. **Settling time**
   
The settling time defines the time between when a command is issued to a DAC and the time when the output voltage reaches a certain percentage of the final value.

4. **Output voltage**
   
The output voltage of the DAC is usually set by the reference voltage. DACs may either accept an externally supplied reference voltage or may produce a reference voltage
internally. As such, it may be easier to control the output voltage range when using an external voltage reference, at the expense of complexity and PCB footprint.

4.2.1 Selection criteria/requirements

In order to reduce the effects of noise in the system, a relatively high voltage reference was selected. The voltage reference for the DAC is provided by a Texas Instruments REF5040 device which provides a 4.096 V reference [30]. In order to provide 1 mV resolution, a 12-bit or higher DAC is required, whilst supporting the 4.096 V reference voltage. In addition to these criteria, a DAC with a settling time of 1 µs is required. A Texas Instruments DAC8830 was selected as this part suits the aforementioned criteria [31].

4.2.2 SPI Interface

SPI (Serial Peripheral Interface) is a synchronous serial bus which is often used to interface hosts to peripherals including a wide array of memories (Flash, SRAM and EEPROMs), digital potentiometers, DAC and ADCs. Using a 3-wire interface, bi-directional communications can be achieved.

A sample of a 16-bit communication between the DAC8830 and the host microcontroller is shown in Figure 4.10. A disadvantage of using an SPI interface DAC is that the high frequency clock pulses (16 clocks per data word) introduces noise into the system. This is evident in the plot of the /CS line in Figure 4.10. Without the clock strobing, the trace is very flat, however after each clock there is a disturbance in the /CS voltage trace. This effect can be partially offset by isolating digital and analog supplies and through appropriate supply decoupling.

---

**Figure 4.10:** SPI bus interface timing between Microchip PIC24FJ64GA002 and TI DAC8830
4.3 Power Supply

To create the highest quality films, it is necessary to provide a low noise current source. However, in the interests of cost benefit, the possibility of using a switch mode power supply (SMPS) to provide power to the pulsed current source unit was investigated.

The output noise of the SMPS is shown in Figure 4.11 exhibiting high-frequency noise levels of almost 140 mV<sub>P-P</sub>. The result of powering the pulsed current source using the SMPS (via a 100 μH/2000 μF LC filter) is shown in Figure 4.12.

![Figure 4.11: Output noise on an SMPS measured at almost 140 mV<sub>P-P</sub>](image)

![Figure 4.12: Bottom two traces showing noise and FFT of noise in the output of the pulsed current source using an SMPS](image)

The upper trace shows the system programmed to provide 250 mA current pulses at a frequency of 10 kHz. The trace below shows the output voltage of the SMPS fluctuating up and down is the current load demand changes. As long as the required load voltage is less than the lower limit of the voltage fluctuations, then this is of little concern. Of primary concern is the lower trace (above the FFT) which shows the current noise which is superimposed on the output current pulses. This voltage is measured across the 1 Ω
test load, thus representing a $20 \, \text{mA}_{pp}$ current noise amplitude – a large proportion of the $250 \, \text{mA}$ programmed current pulse amplitude. Similar results were obtained for $500 \, \text{mA}$ current pulses. Such noise amplitudes are unacceptable and indicate that the use of SMPS supplies to provide power for PS anodisation is not a suitable solution.

The excessive noise in the output can be attributed to difficulty in removing high-frequency noise. The presence of such high-frequency noise is shown in the FFT plot of Figure 4.12, with the peak of the noise spectrum centred on the SMPS switching frequency of around 375 kHz, extending with substantial amplitude into its harmonics. This problem is not uncommon and many commercial products also exhibit similar problems in attenuating high-frequency noise, as shown in Figure 4.13.

![Ripple Rejection graph](image)

*Figure 4.13: A significant reduction in PSRR is experienced on many regulation devices, such as the National Semiconductor LM317 voltage regulator, from [25]*

### 4.4 Complete Pulsed Current Source

The final pulsed current source schematic diagram is shown in Appendix 9.1.

*Figure 4.14 shows the assembled final PCB for the pulsed current source with each subsystem physically separated in an attempt to reduce crosstalk from each system contaminating the sensitive analog section with noise.*

To further reduce noise which may be induced in the analog circuitry, three separate ground traces (power, digital and analog) are combined together at a single star earthing point, as shown in Figure 4.15.
Figure 4.14: Assembled PCB for the pulsed current source showing separation of circuit systems to prevent noise

Figure 4.15: The use of a star earthing point helps to prevent digital return signals contaminating the analog ground trace with noise

Figure 4.16 shows the rise and fall time of the output current signal for an output current of 250 mA. For each oscilloscope plot, the upper trace shows the output voltage from the DAC8830 while the bottom trace shows the voltage measures across the current sense resistor which is approximately proportional to the current through the load. The plot demonstrates the system’s ability to provide a 384 ns rise time and a 380 ns fall time which surpasses the 1 μs requirement stipulated by the target specifications.
The spikes which can be seen before the rise in the output current waveform are caused by digital switching noise due to communications between the microcontroller and the DAC chip in order to update its programmed output value. Better supply filtering and supply isolation, especially in the ground traces may prove to be beneficial in reducing this noise.

*Figure 4.17* shows the system at the worst-case target speed and current operating conditions: providing a 1.5 A current pulse at a frequency of 10 kHz and a duty cycle of 10% into a 10 Ω load. It is clear that the supply has been able to achieve this target specification. Despite providing current pulses with amplitude six times that of those used in the oscilloscope performance plots in *Figure 4.16*, the system maintains a rise time of just under 1 μs and a fall time much better than the 1 μs specification.
4.4.1 Noise Reduction

Despite efforts to reduce noise in the output current waveform, levels of around 20 mA (RMS) existed across the programmable current range, shown in Figure 4.18. Although this is not significant at high current levels (representing only 1% of the maximum design output current), it is significant for smaller currents which may be programmed into the system.

![Figure 4.18: Noise on output waveform when producing a 250 mA output current measured at around 19 mA\textsubscript{RMS} when using a 1 \Omega current sense resistor](image)

By increasing the current sense resistor to 10 \Omega, significantly reduced noise amplitude can be realised at the expense of reducing the maximum output voltage limit. Figure 4.19 shows the effect of the higher resistance value where the voltage produced by the current noise remains the same, which reflects a 10-fold decrease in the output noise level to just over 600 \mu A (RMS).

![Figure 4.19: Noise on output waveform when producing a 250 mA output current measured at around 6.27 mV/\text{R}_s = 627 \mu\text{A}_{\text{RMS}} when using a \text{R}_s = 10 \Omega current sense resistor](image)
5 Monitoring Systems

The monitoring system is designed in an attempt to help better understand the electrochemical reaction that occurs during the anodisation of PS. In order to achieve this, the monitoring system provides facilities to measure and record the voltage which appears across the PS sample throughout the anodisation process.

5.1 Analog to Digital Conversion

The purpose of analog to digital conversion is to provide the system with a digital (i.e. numerical) representation of the analog voltage which appears across the PS load during the anodisation process.

5.1.1 Part Selection

There are many different criteria which may be used to decide the appropriateness of a ADC of a particular application. Two specifications are of particular significance to the use of a ADC in this particular application.

1. Resolution

The ADC resolution determines the voltage step of a single ADC quantisation step. This concept is similar to that discussed for a DAC in Chapter 4.2. The size of each step for a unipolar (only positive or negative voltages) ADC output can be found using Equation (5.1).

\[
\Delta V = \frac{V_{\text{ref}}}{2^n}
\]  

(5.1)

2. Sample rate

The sample rate defines the maximum rate at which the ADC can sample the data and convert this value to a digital representation.

Selection of an ADC was simplified due to the relaxed design criteria to simply better the current system in use at The University of Western Australia which provides a sample rate of around 100 samples per second (SPS) and accuracy of around 5 mV. The Texas Instruments ADS8330 was selected due to its ability to better the aforementioned design criteria [32]. Its dual input design also facilitates the option to monitor both voltage and current by only changing the monitoring system’s firmware.
5.2 Signal Conditioning

Due to the design of the pulsed current source, as discussed in Chapter 3, a high common mode voltage may exist across the load, although the voltage across the load itself may only be very small. In order for anodisation voltage to be measured, the common mode voltage must be removed which will allow the differential voltage to be obtained. The process to achieve this is discussed in Chapter 5.2.1. Further, due to the use of a single rail power supply, it is necessary to provide certain compensation mechanisms to ensure that voltages from the operational amplifiers do not approach the ground rail as this may lead to measurement errors, particularly if the operational amplifier is not characterised as a rail-to-rail device. This is discussed in Chapter 5.2.2.

Finally, an anti-aliasing filter must be used before the anodisation voltage is quantised. The design of this filter is discussed in Chapter 5.2.3.

5.2.1 Common Mode Voltage Rejection

Figure 5.1 shows the differential voltage which the system wishes to measure: the voltage across the load connected across the connector, P1, which is equal to:

\[ V = (V_s +) - (V_s -) \]  

(5.2)

However this voltage is offset from ground by a common-mode voltage, \( V_{CM} \):

\[ V_{CM} = (V_s -) \]  

(5.3)

In order to extract the differential voltage (which may be quite small in comparison to the common-mode voltage), a differential amplifier can be used. An implementation of this is shown in Figure 5.2.
5.2.2 Zero Offset Compensation

Ideally, for $V_{s+} = V_{s-}$, then the output voltage will be zero, however due to practical limitations of operation amplifiers, the output voltage is limited to some finite level from the voltage supply rails. That is, when the operation amplifier is configured using a single-rail supply, then the minimum output voltage is limited to some voltage above 0 V.

This issue was resolved by offsetting the output voltage by a fixed amplitude to ensure that the output voltage never reaches zero. Subsequent processing can then be used to remove the fixed (and thus known) offset to restore the actual differential voltage reading. This system is shown in Figure 5.3. This comes as the expense of a small loss in the dynamic range of the voltage measurement and thus a small loss in the potential quantisation resolution of the ADC.
Figure 5.2: A differential amplifier can be used to remove common-mode voltage however output voltage limitations of the operation amplifier may result in errors

Figure 5.3: A known offset can applies which ensures that the output voltage limitations of Figure 5.2 never occur

Although the 4.096 V reference is used to provide the differential amplifier offset, a mismatch in the ratio between the internal 25 kΩ resistor pairs in the INA2133 difference amplifier may result in a small gain in the offset voltage. Consequently, in order to remove the offset voltage from the ADC reading, it is necessary to determine the value of the offset. This is performed using a calibration command which reads the ADC value while the supply is switched off and the output terminals are shorted. This value is then stored and is subtracted from ADC readings to obtain the original ADC voltage measurement.
5.2.3 Antialiasing Filter

When sampling an analog signal, input frequency components exceeding the Nyquist frequency (defined as half the sampling rate) are aliased to below the Nyquist rate [33]. In order to prevent corruption of the signal being sampled, it is necessary to remove these high frequency components prior to sampling. This can be achieved through the use of an anti-aliasing filter, that is, a low-pass filter (LPF).

A 12.5 kHz cut-off frequency was selected in light of the fact that the monitoring system is expected to be operated in excess of 100 kSPS (providing a Nyquist frequency of 50 kHz, or twice the design cut-off frequency). Due to the application of square current waveforms when using pulsed current anodisation, a filter with a linear phase response was desirable. An 8th-order Bessel LPF was therefore designed using Texas Instruments’ FilterPro software [34]. The result of this design is shown in Figure 5.4.

![Figure 5.4: Schematic of the 8th-order Bessel anti-aliasing filter used for the ADC, as designed with the aid of Texas Instruments’ FilterPro software.](image)

Figure 5.5 shows the frequency and phase response of the filter shown in Figure 5.4. The almost flat group delay up to the design cut-off frequency of the Bessel filter can be seen while the relatively slow rate of high-frequency attenuation is also visible.

A MATLAB simulation of the filter and ADC suggests that a signal-to-noise ratio (SNR) of around 74 dB can be achieved. Using Equation (5.4), it can be seen that this SNR can provide up to 12-bits if quantisation resolution (ENOB). This is short of the 15-bits required to achieve the 1 mV desired resolution when using a 4.096 V reference, as
defined by *Equation* (5.1). However, as shown in *Figure 5.6*, the application of a square current waveform may not necessarily result in a square output voltage waveform. This means that the output voltage waveform has significantly lower high-frequency components that that calculated in the MATLAB simulation and thus a higher SNR can be achieved. The performance of the filter will therefore depend on the exact voltage waveforms which are produced.

\[
\text{ENOB} = \frac{\text{SNR} - 1.76}{6.02}
\]

(5.4)

*Figure 5.5*: Frequency response of the anti-aliasing filter, characterised by a 12.5 kHz cut-off frequency and a maximally flat group delay in the pass-band

*Figure 5.6*: Application of a square current waveform may not necessarily result in a square output voltage waveform, from [21]
5.3 PC Interface

Connection of the monitoring unit to a host PC is provided by a high speed serial link, emulated over a USB connection. The use of a serial connection from the microcontroller simplifies firmware development while USB emulation ensures that connectivity can be achieved using almost any PC with a USB port.

5.3.1 Communications Protocol

To provide maximum system flexibility, communication between the host PC and the host microcontroller takes place using standard 9600 baud serial, with 8 data bits and 1 stop bit. This format is supported by many generic PC terminal programs which means that it is not necessary for users to use the PS Anodisation Control (PSAC) program to control most of the system’s functions. The only function which is not supported using the 9600 baud serial connection is the transmission of logging data. When this mode is selected, the system automatically changes to provide a 2 MBaud serial connection to provide a higher data bandwidth which can support live streaming of 16-bit ADC data at a rate in excess of 150 kSps.

The entire command set, including the packet header, is encoded in plain-text (human-readable) ASCII. This helps to further maintain functionality with generic terminal programs by allowing command to be typed into the terminal program using a standard PC keyboard. The only data which does not appear in plain-text format is the ADC monitoring data due to the high bandwidth requirements which would otherwise be required for readable ASCII representations of the data to be sent.

Reliable system communication is provided through packet framing and packet checksums. In the case of a suspected loss of frame synchronisation, the host PC attempts to flush the host microcontroller’s serial input buffers before attempting to reconnect and resynchronise with the host microcontroller.

The complete communications protocol is described in the document in Appendix 9.3.
6 Automation System

In order to facilitate the widespread use of PS optical filters, it is important to ensure that it is possible to reliably reproduce complex PS structures. This project aimed to achieve this through the design of an automation system which provides computerised control over the whole anodisation process. This includes automatic setting of etch current properties (such as current amplitude, frequency and duty cycle), as well as control over the gantry module.

6.1 Automation Control Interface

Automation functions are provided through the PSAC program under the Automation tab. This is shown in Figure 6.1. In this case, the system is programmed to provide a sequence of different current waveforms for a specific period of time.
6.2 Method of Operation

The automation system first calculates the time at which each event in the sequence should occur. In the case of a command which is to be sent to a peripheral module, the time at which the command should be sent is calculated and the command code is determined. In the case of a delay, no command code is determined, but the time of the next automation command is incremented by the specified delay period. The program then executes each of the steps at the calculated time and transmits commands to the host controller as necessary.

6.3 Testing

The automation listing shown in Figure 6.1 describes an output current waveform as follows:

1. 200 mA amplitude at 5 Hz, 50% for 1 second
2. No output for 1 second
3. 100 mA amplitude at 5 Hz, 50% for 1 second
4. 100 mA amplitude at 10 Hz, 50% for 1 second

The output current waveform produced using the automation program shown in Figure 6.1 is shown in Figure 6.2. It can be seen that the waveform follows quite closely with the expectation, as outlined above. Minor discrepancies between the expected number of pulses (eg. Current pulses at 5 Hz for 1 second should result in 5 pulses) exist. This can be attributed to communication latencies and the processing of commands with respect to the state of the current source microcontroller’s interrupt timers.

Figure 6.2: Output current waveform produced from the automation program shown in Figure 6.1, with a zoom of the high frequency region (bottom trace)
6.4 Automation System Timing Error

With a delay period of one second, the 10 Hz part of the process should result in exactly 10 current pulses. Close examination of the 10 Hz pulses shows an extra 1 or 2 current pulses than expected, representative of a delay of 0.1 to 0.2 seconds.

In order to ensure communication system synchronisation, a delay of 50 ms is placed between commands. This proves to be a significant source of timing error.

With a command packet length of 16 bytes and at a rate of 9600 baud, communications introduces a delay of at least 16.7 ms. Ignoring the latencies associated with the host microcontroller forwarding packets to the peripheral units (which is in the order of hundreds of nanoseconds), then delays associated with the two hop process for data to reach the peripheral is at least 33.3 ms.

Ultimately, almost all of the timing error can be attributed to timing delays arising from the communication interfaces:

1. Synchronisation pause delay
2. The link between the PC (and the PSAC automation screen) to the host microcontroller
3. The link between the host microcontroller and the peripheral module controller (in this case, the current source module microcontroller)

Furthermore, it can be seen that the synchronisation delay is the most significant source of error. However with anodisation times which are much longer than the period of the error, this is unlikely to have any serious repercussion on the PS films which are produced. Shorter anodisation times can also be adjusted according to these error times to minimise the impact of these errors.
7 Conclusion

To motivate this project, optical modelling software has been developed which has been used to demonstrate the effects of porosity gradients and interface roughness on the performance of PS optical filters. Based upon these results, it is evident that significant improvements in filter performance can be achieved by controlling these imperfections which occur during conventional DC anodisation techniques.

To that end, this project has successfully designed, built and tested a high-speed and high-precision pulsed current source. It has demonstrated low noise characteristics which should be suitable for use in the anodisation of high-quality PS optics. It also has the ability to produce high-frequency current pulses which can be used to investigate the effects of high-frequency anodisation and the dramatic increase in interface roughness which has been observed to stem from it.

To help better understand the formation of pores in PS, an electrochemical potential monitoring unit has also been designed and constructed. As the monitoring unit which is currently in use has provided only limited electrochemical potential information, it is difficult to assess quantitatively the extent of the additional insight that can be gained from the use of this new system. However the specification of the new unit significantly surpasses that of the existing unit and therefore has the potential to provide a plethora of new information to researchers at The University of Western Australia.

An automation unit has been also been developed. This will aid in the production of complex multilayered PS structures, such as those required for PS optical filters, while maximising the reproducibility of the results.
8 Future Work

8.1 High Frequency Pulsed Current Anodisation
The pulsed current supply designed and built as part of this project is capable of providing high frequency current pulses and thus work can now be performed to investigate whether the trend of using high frequency pulses resulting in high interface roughness continues beyond the current research limit of 1 kHz.

The external signal input also paves the way for investigation into the use of arbitrary anodisation current waveforms to be used for the anodisation of silicon wafers.

8.2 Modelling and Anodisation Systems Integration
The PS modelling software developed as part of this project currently exists as a completely separate piece of software from the PSAC program. It may be possible to bring together the two applications into a unified application which allows users to design a PS optical filter and then directly export the design to the anodisation systems in order to produce a real-world product.

This would require the development and implementation of models which relate physical parameters (such as porosity and etch rate) to anodisation parameters (such as current density and time).

8.3 Embedded Monitoring
Due to the space confined environment within a cleanroom, it may be ideal to incorporate the entire monitoring unit within the embedded system. That is, it may be possible to add a Flash memory system to the current monitoring unit to eliminate the need to stream data back to an attached PC. Such as system may store data to Flash memory such as an Secure Digital (SD) card and would ideally utilise a file system (such as FAT32) to enable easy copying of the monitoring data to a PC outside the cleanroom after the anodisation process has been completed.

8.4 Low Temperature Growth
The importance of high interface quality was also expressed by Setzu et al. [3] where the effects of anodisation temperature were related to interface roughness. Their results
showed that roughness can be reduced by a factor of six at low current densities by reducing the temperature from +26 °C to -35 °C, as shown in Figure 8.1, while smaller but significant reductions are still realised at higher current densities. The reduction in roughness at low temperatures was attributed to higher electrolyte viscosity. This increases the rate of electropolishing which smooths the interfaces resulting in lower interface roughness [3]. The importance in reducing interface roughness is discussed by Setzu et al. [13] where a “reduction in the light diffusion by a factor of 18” was observed.

![Figure 8.1: Effect of temperature on interface roughness, from [3]](image-url)
# Appendix

9.1 Pulsed Current Source Schematic and PCB Artwork ........................................... 66
9.2 Monitoring Unit Schematic and PCB Artwork ...................................................... 69
9.3 Host Controller Communication Protocol and Command Set ............................. 74
9.4 MATLAB Optical Modelling Program ................................................................ 79  
  9.4.1 ema_s: Effective Medium Approximations .................................................. 79
  9.4.2 normreflect: Normal Reflection ...................................................................... 80
  9.4.3 reflect_s: Reflection ..................................................................................... 81
9.1 Pulsed Current Source Schematic and PCB Artwork
Linear Pulsed Current Source
Yang Li, PHAY (2014/05/1)
Final Year Project, Adrian Kesting

[Diagram of a circuit board showing components and labels]

Current Control and Monitoring for High Quality Porous Silicon Optics
9.2 Monitoring Unit Schematic and PCB Artwork
Current Control and Monitoring for High Quality Porous Silicon Optics
9.3 Host Controller Communication Protocol and Command Set

The following document is found as an attached application note for peripherals which connect to the host microcontroller.
PS Anodisation Controller Command Set

The following outlines the communications protocol and command set of the PS Anodisation Controller.

Physical and Link Layers

The primary controller interfaces to a PC via a USB connection with a FT232R USB UART chip. In order to perform basic controller functions, the FTDI CDM drivers are required, however to perform high speed communications as required by the monitoring unit during sampling, the FTDI D2XX drivers are required.

Commands (PC to/from controller)

All commands (except for administration of the monitoring data stream) are sent to and from the primary controller according to the following serial protocol:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>9600 baud</td>
</tr>
<tr>
<td>Data bits</td>
<td>8</td>
</tr>
<tr>
<td>Stop bits</td>
<td>1</td>
</tr>
<tr>
<td>Parity</td>
<td>None</td>
</tr>
</tbody>
</table>

Monitoring Data (controller to PC)

The baud rate for the streaming of monitoring data can be chosen via the monitoring unit’s RUN command to be any one of the following:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>9600 baud, 38.4 kbaud, 2.0 Mbaud</td>
</tr>
<tr>
<td>Data bits</td>
<td>8</td>
</tr>
<tr>
<td>Stop bits</td>
<td>1</td>
</tr>
<tr>
<td>Parity</td>
<td>None</td>
</tr>
</tbody>
</table>

Commands (controller to/from peripherals)

Communications from the primary controller to the peripheral modules (eg. Current source controller and gantry) follow the same communications protocol as used for normal command communications between the PC and primary controller, namely:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>9600 baud</td>
</tr>
<tr>
<td>Data bits</td>
<td>8</td>
</tr>
<tr>
<td>Stop bits</td>
<td>1</td>
</tr>
<tr>
<td>Parity</td>
<td>None</td>
</tr>
</tbody>
</table>
Network and Transport Layers

All commands are transmitted in 16-byte packets using the aforementioned physical layer communication criteria. The command packet is shown below:

<table>
<thead>
<tr>
<th>SYNC</th>
<th>SYNC</th>
<th>MODULE</th>
<th>MODULE</th>
<th>COMMAND</th>
<th>COMMAND</th>
<th>OPCODE</th>
<th>OPCODE</th>
<th>OPCODE</th>
<th>OPCODE</th>
<th>OPCODE</th>
<th>OPCODE</th>
<th>OPCODE</th>
<th>CHECK</th>
<th>TERMINATION</th>
</tr>
</thead>
</table>

SYNC

Two synchronisation bytes are used to statistically delineate the frame packet. The two bytes are defined as ‘U’ (0x55).

MODULE

Three bytes are used to indicate the target module of the command packet and are used by the primary controller in the forwarding of command packets to the correct peripherals. Valid module codes are the monitor (MON), current source (SRC), gantry (GTY), programming (PGM) and configuration (CFG) modules.

COMMAND

Three bytes are used for a command descriptor.

OPCODE

Six bytes are used as operation codes or parameters for the command.

CHECK

One byte is used as a checksum for the command packet. The checksum byte can be computed by summing the numerical ASCII code for the SYNC, MODULE, COMMAND and OPCODE bytes together and wrapping this number around the 26 uppercase characters in the alphabet (‘A’ through ‘Z’). Example code in Visual Basic and C are shown over the page.

TERMINATION

One termination byte is used to indicate the end of the command. The single byte is defined as <CR> (0x0D).
**Visual Basic (VB .NET 2008)**

```vbnet
Function _commsChecksum(ByVal cmd As COMMAND) As String
    Dim cSync, cModule, cCommand, cOpcode As Integer
    Dim sum As Integer
    cSync = Asc(cmd._sync(0)) + Asc(cmd._sync(1))
cModule = Asc(cmd._module(0)) + Asc(cmd._module(1)) + 
    Asc(cmd._module(2))
cCommand = Asc(cmd._command(0)) + Asc(cmd._command(1)) + 
    Asc(cmd._command(2))
cOpcode = Asc(cmd._opcode(0)) + Asc(cmd._opcode(1)) + 
    Asc(cmd._opcode(2)) + Asc(cmd._opcode(3)) + 
    Asc(cmd._opcode(4)) + Asc(cmd._opcode(5))
    sum = (cSync + cModule + cCommand + cOpcode) Mod 65 + 65
    _commsChecksum = Chr(sum)
End Function
```

**C (Microchip C30)**

```c
char sbuf[16];
int checksum = 0;
GetPacket(sbuf);
for(i=0; i<14; i++) {
    checksum = checksum + (int)sbuf[i];
}
checksum = (checksum % 26) + 65;
```

**Acknowledgement**

Upon receipt of a command, the checksum should be verified and an acknowledgement byte should be returned. A single acknowledgement byte of the received checksum character should be returned.

**Application Layer**

Commands should be parsed and verified according to structure described in the Network and Transport Layers to produce a command and operational code for use by the peripheral controller. The command set for each module is outlined below. Any numerical operational codes or parameters should be right adjusted (eg. the number 16 is represented as 000016).

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAM</td>
<td>Set sample rate</td>
<td>Sample rate in samples per second</td>
</tr>
<tr>
<td>RUN</td>
<td>Start sampling</td>
<td>Sample data streaming baud rate (0 for 2 Mbaud)</td>
</tr>
<tr>
<td>STP</td>
<td>Stop sampling</td>
<td><em>None</em></td>
</tr>
<tr>
<td>BUF</td>
<td>Use buffer</td>
<td>0 for no buffer, non-zero to use buffer</td>
</tr>
<tr>
<td>ULD</td>
<td>Upload buffer</td>
<td>Upload baud rate (0 for 2 Mbaud)</td>
</tr>
</tbody>
</table>

**PS Anodisation Controller Command Set**

Version: 0.1 (18 August 2009, YLP)
### Current Source (SRC)

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIG</td>
<td>Set high current</td>
<td>Current in milliamps (mA)</td>
</tr>
<tr>
<td>LOW</td>
<td>Set low current</td>
<td>Current in milliamps (mA)</td>
</tr>
<tr>
<td>DTY</td>
<td>Set duty cycle</td>
<td>Duty cycle in percent (%)</td>
</tr>
<tr>
<td>FCY</td>
<td>Set frequency</td>
<td>Frequency x 10 (Hz)</td>
</tr>
<tr>
<td>TYP</td>
<td>Set waveform type</td>
<td>“SQR” or “SIN”</td>
</tr>
</tbody>
</table>

### Gantry (GTY)

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>INI</td>
<td>Initialise gantry</td>
<td>None</td>
</tr>
<tr>
<td>MVX</td>
<td>Move x axis</td>
<td>Absolute position from home</td>
</tr>
<tr>
<td>MVZ</td>
<td>Move z axis</td>
<td>Absolute position from home</td>
</tr>
<tr>
<td>SPX</td>
<td>Step x axis</td>
<td>Steps from current location</td>
</tr>
<tr>
<td>SPZ</td>
<td>Step z axis</td>
<td>Steps from current location</td>
</tr>
<tr>
<td>SAV</td>
<td>Save location</td>
<td>Memory location number</td>
</tr>
<tr>
<td>RCL</td>
<td>Recall location</td>
<td>Memory location number</td>
</tr>
<tr>
<td>STA</td>
<td>Get status</td>
<td>None</td>
</tr>
<tr>
<td>HOM</td>
<td>Move to home</td>
<td>None</td>
</tr>
<tr>
<td>STP</td>
<td>Stop gantry</td>
<td>None</td>
</tr>
</tbody>
</table>

### Programming (PGM)

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN</td>
<td>Start program</td>
<td>None</td>
</tr>
<tr>
<td>RST</td>
<td>Reset program</td>
<td>None</td>
</tr>
<tr>
<td>RCL</td>
<td>See Gantry</td>
<td>None</td>
</tr>
<tr>
<td>DTY</td>
<td>See Current Source</td>
<td>None</td>
</tr>
<tr>
<td>FCY</td>
<td>See Current Source</td>
<td>None</td>
</tr>
<tr>
<td>HIG</td>
<td>See Current Source</td>
<td>None</td>
</tr>
<tr>
<td>LOW</td>
<td>See Current Source</td>
<td>None</td>
</tr>
</tbody>
</table>

### Configuration (CFG)

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>None specified</td>
<td></td>
</tr>
</tbody>
</table>
9.4 MATLAB Optical Modelling Program

The following code is that which is used by the PSAnalysis program to model the optical properties of PS films.

9.4.1 ema_s: Effective Medium Approximations

This function is used to convert porosity to a refractive index.

```matlab
function ema(n_si, EMAmethod, por)

n_air = 1;
%n_si = 3.5;
e_air = n_air^2;
e_si = n_si^2;

%MGT EMA
if (strcmp(EMAmethod, 'mgt') ~= 0)
    %disp('mgt')
    mgt = e_si*(1-(3*por*(e_si-e_air))/(e_air+2*e_si-por*(e_air-e_si)));
    refind = sqrt(mgt);
end

%Bruggeman EMA
if (strcmp(EMAmethod, 'brug1') ~= 0)
    %disp('brugg')
    syms e_eff
    brugpoly = e_eff^3 - (3*(e_air^2))*(e_eff^2) + ((3*(e_air^2))-(1-por)^3)*(1/e_si)*((e_air-e_eff)^3)*(e_eff)-e_air^3;
    brugcoeff = sym2poly(brugpoly);
    r = roots(brugcoeff);
    brug = r(1);
    refind = sqrt(brug);
end

%Bruggeman EMA
if (strcmp(EMAmethod, 'brug2') ~= 0)
    %disp('brugg')
    syms e_eff
    brugpoly = e_eff^3 - (3*(e_air^2))*(e_eff^2) + ((3*(e_air^2))-(1-por)^3)*(1/e_si)*((e_air-e_eff)^3)*(e_eff)-e_air^3;
    brugcoeff = sym2poly(brugpoly);
    r = roots(brugcoeff);
    brug = r(1);
    refind = sqrt(brug);
end

%VAT EMA
if (strcmp(EMAmethod, 'vat') ~= 0)
    %disp('vat')
    vat = (1-por)*e_si+por*e_air;
    refind = sqrt(vat);
end

disp(refind)
```
9.4.2 normreflect: Normal Reflection

This function is used to determine the reflectivity spectra of a thin film assembly and also applies porosity gradient and roughness parameters.

```matlab
function [h] = normreflect(matprop, lamdaparam, roughness, gradient)
% matprop = [optindex thickness(nm) ; ... ; optindex thickness(nm)]
% lamdaparam = [start_wavelength(nm) delta_wavelength(nm) end_wavelength(nm)]
% roughness = roughness(nm)
% gradient = [type rate ratetype steps]

% Setup range of wavelengths to computer reflectivity data
wavelengths = lamdaparam(1):lamdaparam(2):lamdaparam(3);

matpropstruct = [0 0];
pergrad = gradient{2}/100;
pergrad = pergrad / ((size(matprop,1)-1) * gradient{4});

% Create new structure to add new layers representing the porosity gradient
for i=0:size(matprop,1)-1
    % Convert percentage gradient into an absolute number (gradient across the layer)
    if(strcmp(gradient{3},'percent') ~= 0)
        absgrad = (gradient{2}/100) * matprop(i+1,1);
    else
        absgrad = gradient{2};
    end
    absgrad = absgrad / size(matprop,1);

    for j=0:gradient{4}-1
        if(strcmp(gradient{1},'linear') ~= 0)
            % Set effective refractive index for this step
            matproplayer(1) = matprop(i+1,1) * (1 + (i*gradient{4} + j)*pergrad);
        end
        if(strcmp(gradient{1},'exp') ~= 0)
            % Set effective refractive index for this step
            matproplayer(1) = matprop(i,1) + (absgrad/matprop(i,2))*(j*(matprop(i,2)/(gradient{4}-1)));
        end
        if(matprop(i+1,1) == 3.5)
            matproplayer(1) = 3.5;
        end
        matproplayer(1) = min(matproplayer(1), 3.5);

        % Set layer thickness for this step
        matproplayer(2) = matprop(i+1,2)/gradient{4};
        matpropstruct = cat(1, matpropstruct, matproplayer);
    end
end

matpropstruct(1,:) = []
```
% Compute the reflectivity of the structure at each wavelength sample point
for n=1:size(wavelengths,2)
    % Standard reflection calculation according to Fresnel's equations
    reflectance(n) = reflect_s(matpropstruct,wavelengths(n));

    % Compensation for roughness
    reflectance(n) = reflectance(n) * exp(-
        (4*pi*roughness/wavelengths(n))^2);
end

h = plot(wavelengths,reflectance);

9.4.3  reflect_s: Reflection
This function is used to determine the reflectivity of a thin film assembly at a particular wavelength.

function R = reflect_s(matprop,wavelength)
% matprop = [optindex thickness ; ...; optindex thickness]
% Convert refractive indexes into optical admittances
% Admittance = refractive index * admittance of free space (admitFS)
admitFS = 1/377;
admit = matprop(:,1) .* admitFS;

% Calculate phase change for each layer
% McLeod p33, eq(2.54)
phasedelta = 2*pi.*matprop(:,1).*matprop(:,2)/wavelength;

% Setup EM-field at substrate boundary and apply characteristic matrix
% McLeod p33, eq(2.48-2.49,2.55)
% [E;H]=[E;admittance*E]
emB = [1 ; admit(size(matprop,1))];
emA = M*emB;

% Determining system admittance
% McLeod p34, eq(2.56)
% Y = Ha/Ea, Ea = emA(1) Ha = emA(2)
Y = emA(2) / emA(1);

% Use system admittance to determine reflectance
% McLeod p34, eq(2.57)
R = ((admitFS - Y)/(admitFS + Y)) * conj((admitFS - Y)/(admitFS + Y));
10 References


